## I. SVX4 Configuration Register Table

| Bit Number | Bit Name | Description | Values | Nominal Setting |
|---|---|---|---|---|
| **— Frontend Bit Assignments —** | | | | |
| 0:127 | Mask [127:0] | Cal mask or channel disable register (see next bit assignment) | 0 = mask/enable<br>1= unmask/disable | 0 .. 0 |
| 128 | Disable | Select whether mask reg acts as a channel disable reg or a cal mask reg | 0 = cal mask<br>1= channel disable | 0 |
| 129:132 | BW [0:3] | Preamp risetime adjustment (depends on input capacitance), binary weighted | For Cin=10 pF:<br>Tr ≈ 25 nS + (BW * 4 nS)<br>For Cin=50 pF:<br>Tr ≈ 60 nS + (BW * 10 nS) | 0010 |
| 133:136 | Isel [0:3] | Preamp input FET bias current adjustment, binary weighted | Bias current ≈ 164 uA + (Isel * 32 uA) | 0010 |
| 137:138 | IWsel [0:1] | Pipeline write amp bias current adjustment, NOT binary weighted | Bias current ≈ 26 uA + (IWsel0 * 26 uA) + (IWsel1 * 26 uA) | 10 |
| 139:140 | IRsel [0:1] | Pipeline read amp bias current adjustment, binary weighted | Bias current ≈ 26 uA + (IRsel * 13 uA) | 10 |
| 141:146 | PickDel [0:5] | Trigger latency; select system L1A delay as a number of FEClk periods | 0 .. 42 | TBD |
| 147 | PB | Pipeline readout order | 0 = pedestal, signal<br>1 = signal, pedestal | 0 |
| **— Backend Bit Assignments —** | | | | |
| 148:154 | ID [6:0] | Chip ID assignment | 0 .. 127 | TBD |
| 155 | RTPS | Real Time Pedestal Subtraction disable | 0 = RTPS on<br>1 = RTPS off | 0 |
| 156 | Rd127 | Always readout channel 127 regardless of hit status | 0=Rd127 off<br>1 = Rd127 on | 0 |
| 157 | Rd63 | Always readout channel 63 regardless of hit status | 0=Rd63 off<br>1 = Rd63 on | 0 |
| 158 | RdAll | Always readout all channels | 0=RdAll off<br>1 = RdAll on | 0 |
| 159 | RdNeigh | Readout hit channels and their neighbors | 0=RdNeigh off<br>1 = RdNeigh on | 1 |

| Bit Number | Bit Name | Description | Values | Nominal Setting |
|---|---|---|---|---|
| 160:163 | RampPed [0:3] | ADC ramp pedestal setting, binary weighted | RampDir=0: Ped ≈ 480 mV +(RampPed * 23 mV)<br>RampDir=1: Ped ≈ 1.8 V -(RampPed * 23 mV) | 0001 |
| 164 | RampDir | ADC ramp direction, ramp up or ramp down | 0 = ramp up<br>1 = ramp down | 0 |
| 165 | CompPol | Comparator polarity; sets comparator and delay input for 0→1 or 1→0 transition | 0 = 0→1 (for RampDir=0)<br>1 = 1→0 (for RampDir=1) | 0 |
| 166:168 | RampRng [0:2] | ADC ramp range, adjusts slope of ramp | Slope ≈ 0.5 mV/nS * $[1+(4*r0)+(3*r1)+(1*r2)]^{-1}$ | 000 |
| 169:176 | Thresh [7:0] | ADC digital threshold setting, Gray code | 0 .. 255 | TBD |
| 177:184 | CntrMod [7:0] | Counter Modulo, sets counter value at which overflow occurs, Gray code | 0 .. 255 | TBD |
| 185 | FC | First Chip flag; enables the first chip to drive OBDV before readout begins | 1 = this is the first chip | 0 |
| 186 | LC | Last Chip flag; enables the last chip to drive OBDV after readout ends | 1 = this is the last chip | 0 |
| 187:189 | DriverI [2:0] | Output driver current select; selects output series resistance; the resistance selected appears in series on EACH output pin (plus and minus) | $R \approx [(d2/43) + (d1/86) + (d0/172)]^{-1}$<br><br>Drivers off if DriverI = 0 | 111 |

Notes:
1) The correspondence of the bus notation indicies are preserved in the table above from column-to-column, i.e. for "Bit Number 160:163," RampPed [3] corresponds to Bit 163, which corresponds to a "1" in the "Nominal Setting" column. This correspondence explicitly determines whether the LSB or MSB of a bus loads first, since there is no common rule.

2) The "Bit Number" references under "Frontend Configuration Register Bit Assignments" are reversed with respect to the "SVX4 Front End" document, in order to accommodate a contiguous, ascending bit order for the complete configuration register.

3) Bit 0 loads first.